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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

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Sheet 1 6

**Complete if Known**

Application Number	10/762,937
Filing Date	January 21, 2004
First Named Inventor	A. MacInnis
Group Art Unit	2628
Examiner Name	Brier, Jeffery A.
Attorney Docket Number	17418US02

**U.S. PATENT DOCUMENTS**

Examiner Initial*	Cite No. <sup>1</sup>	Document Number Number/Kind Code <sup>2</sup> (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/JB/	A1	4,020,332	04-26-1977	Crochiere et al.	
	A2	4,367,466	01-04-1983	Takeda et al.	
	A3	4,532,547	07-30-1985	Bennett	
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	A5	4,688,033	08-18-1987	Carini et al.	
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	A8	4,967,392	10-30-1990	Werner et al.	
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	A10	5,097,257	03-17-1992	Clough et al.	
	A11	5,142,273	08-25-1992	Wobemmin	
	A12	5,155,816	10-13-1992	Kohn	
	A13	5,258,747	11-02-1993	Oda et al.	
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	A17	5,396,567	03-07-1995	Jass	
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	A19	5,404,447	04-04-1995	Drako et al.	
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/Jeffery Brier/

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<sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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Sheet

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Of

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First Named Inventor	A. MacInnis
Group Art Unit	2628
Examiner Name	Brier, Jeffery A.
Attorney Docket Number	17418US02

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JJB	A40	5,625,611	04-29-1997	Yokota et al.	
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Sheet 3 Of 6

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First Named Inventor	A. MacInnis
Group Art Unit	2628
Examiner Name	Brier, Jeffery A.
Attorney Docket Number	17418US02

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JCB	A86	5,959,626	09-28-1999	Garrison et al.	
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	A88	5,960,464	09-28-1999	Lam	
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Sheet 4 Of 6

**Complete if Known**

Application Number	10/762,937
Filing Date	January 21, 2004
First Named Inventor	A. MacInnis
Group Art Unit	2628
Examiner Name	Brier, Jeffery A.
Attorney Docket Number	17418US02

**U.S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. 1	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number/Kind Code 2 (if known)			
/JB/	A132	6,199,131	03-06-2001	Melo et al.	
	A133	6,204,859	03-20-2001	Jouppi et al.	
	A134	6,205,260	03-20-2001	Crinon et al.	
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Examiner Initials*	Cite No. 1	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)				
/JB/	B1	EP 0746116 A2	12-04-1996	Hiratsuka		
	B2	EP 0 752 695	01-08-1997	O'Sullivan		
	B3	EP 0840276 A2	05-06-1998	Benbassat		
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	B8	WO 00/28518	05-18-2000	MacInnis		

**OTHER ART -- NON PATENT LITERATURE DOCUMENTS**

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/JB/	C1	Plaintiff and Counterdefendant Qualcomm Incorporated's Preliminary Invalidity Contentions For U.S. Patent 6,501,480 and 6,570,579, September 1, 2006
	C2	Thomas Porter & Tom Duff, "Compositing Digital Images", Computer Graphics, Vol. 18, No. 3, July 1984, pp. 253-259
	C3	Akeley, K. & Jermoluk T., "High-Performance Polygon Rendering," 22 Computer Graphics No. 4 (ACM August 1988).
	C4	Apgar, B., et al., "A Display System for the Stellar Graphics Superconductor Model GS1000," 22 Computer Graphics No. 4 (ACM August 1988).
	C5	Asai, M.D., et al., "Novel Architecture for a High Performance Full Custom Graphics Processor," (IEEE 1989).
	C6	Awaga, M., et al., "3D Graphics Processor Chip Set," (IEEE December 1995).
	C7	Cox, M. & Bhandari, N., "Architectural Implications of Hardware-Accelerated Bucket Rendering on the PC," (Association for Computing Machinery SIGGRAPH/Eurographics Workshop 1997).
	C8	Cyrix Corporation Manual, copyrighted 1996, 1997, and all underlying development work.
	C9	Deering, M., et al., "The Triangle Processor and Normal Vector Shader: A VLSI System for High Performance Graphics," 22 Computer Graphics No. 4 (ACM August 1988).
	C10	Donovan, W., et al., "Pixel Processing in a Memory Controller," (IEEE Computer Graphics and Applications 1995).
	C11	Dutton, T., "The Design of the DEC 3000 Model 500 AXP Workstation," (IEEE 1993).
	C12	Foley, James D., et al., "Introduction to Computer Graphics," (Addison-Wesley Publishing Co. 1994) ("Introduction to Computer Graphics", pages 141-151.
	C13	Galbi, D., et al., "An MPEG-1 Audio/Video Decoder with Run-Length Compressed Antialiased Video Overlays," (1995 IEEE International Solid-State Circuits Conference).
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	C15	Glaskowsky, Peter, "Intel Displays 740 Graphics Chip: Auburn Sets New Standard for Quality - But Not Speed," Microprocessor Report No. 2, February 16, 1998.
	C16	Gwennap, L., "Verite: A Programmable 3D Chip: Rendition Uses Internal RISC CPU for Versatility, Performance," 10 Microprocessor Report No. 6, May 6, 1996.
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	C19	Lewis, R., et al., "Delivering PCI in HP B-Class and C-Class Workstations: A Case Study in the Challenges of Interfacing with Industry Standards," (Hewlett-Packard Journal May 1998).
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	C22	Norrod, F. & Wawrzyniak, R., "A Multimedia-Enhanced x86 Processor, Digest of Technical Papers," ISSCC96 (February 9, 1996).
	C23	Oguchi, T., et al., "A Single-Chip Graphic Display Controller," (1981 IEEE International Solid-State Circuits Conference).
	C24	Soferman, Z., et al., "Advanced Graphics Behind Medical Virtual Reality: Evolution of Algorithms, Hardware, and Software Interfaces," 86 Proceedings of the IEEE No. 3 (IEEE March 1998 (Manuscript received July 3, 1997)).
	C25	Scott, N., et al., "An Overview of the VISUALIZE fx Graphics Accelerator Hardware," (Hewlett-Packard Journal May 1998) and all underlying development work ("HP").
	C26	Sumi, M., et al., "A 40-Mpixel/s Bit Block Transfer Graphics Processor," (IEEE 1989).
	C27	Foley, James D., et al., Computer Graphics: Principles and Practice; publication, 1996, 1990; The Systems Programming Series, 4 pages, Second Edition in C; Addison-Wesley Publishing Company, U.S.A., pg 585, 886, 838.
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		Attorney Docket Number	17418US02

<b>OTHER ART -- NON PATENT LITERATURE DOCUMENTS</b>		
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
/JB/	C29	Watkins, J., et al., "A Memory Controller with an Integrated Graphics Processor (IEEE 1993).
	C30	Yao, Yong, "Samsung Launches Media Processor: MSP is Designed for Microsoft's New 3D-Software Architecture," 10 Microprocessor Report No. 11, August 26, 1996.
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	C36	Blinn, J., "Compositing, Part I: Theory," (IEEE September 1994).
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	C38	Jaspers, et al., "A Flexible Heterogeneous Video Processor System for Television Applications," (IEEE Sept. 25, 1998).
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	C40	Ostermann, J., "Coding of Arbitrarily Shaped Objects with Binary and Greyscale Alpha-Maps: What Can MPEG-4 Do for You?," (Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 31-June 3, 1998, Vol. 5).
	C41	Stylt, et al., "Three-Dimensional Medical Imaging: Algorithms and Computer Systems," (ACM Computing Surveys, December 1991).
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	C44	Bao, Jay et al., "HDTV Down-Conversion Decoder," IEEE Transactions on Consumer Electronics, pp. 402-410, vol. 42, No. 3, Aug. 1996.
	C45	Mokry, Robert et al., "Minimal Error Drift in Frequency Scalability for Motion-Compensated DCT Coding," IEEE Transactions on Circuits and Systems for Video Technology, pp. 392-406, vol. 4, No. 4, Aug. 1994.
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V	C49	Yu, Haping et al., "Block-Based Image Processor for Memory Efficient MPEG Video Decoding," 1999 IEEE International Conference on Consumer Electronics, pp. 114-115, 1999.

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